Page Faults

75HCT573:
When LOAD is high the latch is transparent (BUSAx will be output to DATAx).
On a high-to-low transition of LOAD the data is latched.

So, we want the default level of LOAD to be low, so it maintains the last latched value. If there is a page fault (FAULT goes low) we want LOAD to briefly go high, then return low, to latch the current address (on bus A). Note that FAULT is not synchronous: as the value of TBLADDR changes we may see transient values on the RAM output, which may lead to an erroneous blip of FAULT, if we don't control for that we'll end up snapping a new address when there was no fault, and losing the last real fault address.

The solution is to NOR FAULT with CLKNARROW. Since CLKNARROW doesn't go low until well after the stabilisation time for the RAM output we shouldn't get false positives.

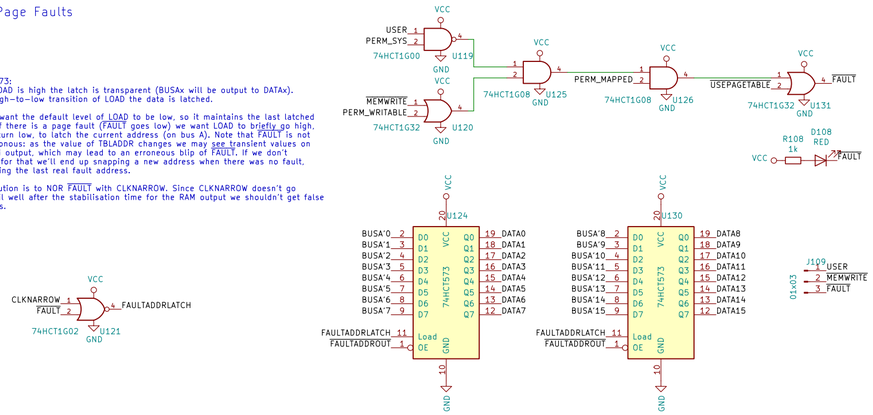


Table Entry/Idx/Perms Output

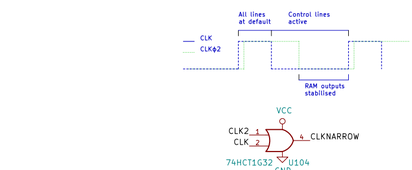
Table RAM

Note: should we have pull-up/down resistors on the TBLENTRY/PERM lines? Otherwise they are floating when OP is 5 or 7, which might cause noise on the FAULT line

Table Address Construction

Physical Address Output

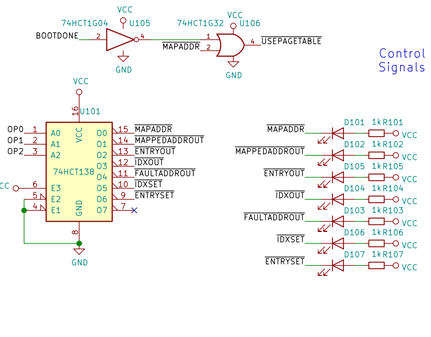
Physical address:
If USEPAGETABLE is low, then TBLENTRY[15..0], BUSA[7..0]
If USEPAGETABLE is high, then 10000000, BUSA[15..0]

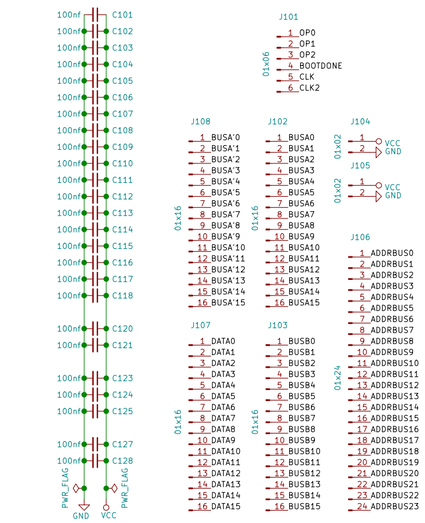


The op codes are structured so that four that need RAM output are 0–3, and the three that don't are 4–6. This means we can use the top bit being low to indicate RAMOUT

OP2 ___ RAMOUT

Control Signals





http://mups16.net/pages/mmu.html
Alistair Potts

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